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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,230	11/26/2003	Hidenori Sato	501.39288CX1	5683

20457 7590 11/10/2004

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EXAMINER	
VESPERMAN, WILLIAM C	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,230	SATO ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/26/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-41* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This action is in response to applicant's filing of 11/26/2003.

Election/Restriction

2. Restriction to one of the following inventions is required under 35 U.S.C. 121.

I. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; (d) forming a plurality of patterns on the semiconductor substrate after step (c); (e) filling a trench forming between the plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method; and (f) filling a remaining portion of the trench into which the third insulating film is filled with a fourth insulating film, wherein the fourth insulation film is more difficult to etch than the third insulating film, wherein step (b) comprises the steps of depositing the first insulating film on a main surface of the semiconductor substrate by a coating method such that the deposited first insulating film has a planarized surface, and then etching back the first insulating film. See embodiment. (Claims 1, 7, 8, 16, 17, 23, 24, 29, 32, 36, 37, 38, 39 and 40 are suggested.)

II. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor

substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; forming dummy patterns in a relatively large isolation region of isolation regions with relatively different planar dimensions before the first insulating film is deposited, wherein the first insulating film is filled into the isolation trenches at the (b) step such that a thickness of the first insulating film is uniform within isolation trenches formed in said isolation regions with relatively different planar dimensions, respectively. See embodiment (Claims 2, 6 and 9 are suggested.)

III. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; (d) forming a plurality of patterns on said semiconductor substrate after insulating film; (d) forming a plurality of patterns on said semiconductor substrate after the step (c); (e) filling a trench forming between the plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film deposited by a coating method; and (f) filling a remaining portion of the trench into which the third insulating film, is filled with a fourth insulating film being more difficult to etch than the third insulating film; and forming dummy patterns in a relatively large

isolation region of isolation regions with relatively different planar dimensions when the isolation trenches are formed. See embodiment. (Claims 3, 30, 33 and 41 are suggested.)

IV. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; forming dummy patterns between said isolation trenches in a relatively Iarge isolation region of isolation regions with relatively different planar dimensions when the isolation trenches are formed such that a planer dimension difference and depth dimension difference of the isolation trenches in the isolation regions with relatively different planar dimensions, respectively, are small. See embodiment. (Claims 4, 31 and 34 are suggested.)

V. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; and forming dummy patterns between said isolation trenches in a relatively large isolation region of isolation regions with relatively different planar dimensions when the isolation trenches are formed such that a planer dimension and

depth dimension of the isolation trenches in said isolation regions with relatively different planar dimensions, respectively are equal in design. See embodiment. (Claim 5 is suggested.)

VI. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming a plurality of patterns, which are adjacent to each other, on a semiconductor substrate; (b) filling a trench formed between the plurality of patterns, which are adjacent to each other, up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; and (c) filling a remaining depth portion of said trench into which the first insulating film is filled with a second insulating film. See embodiment. (Claims 10, 11,12, 14, 15 and 27 are suggested.)

VII. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming a plurality of word lines adjacent to each other on a semiconductor substrate, which form a gate electrode of a field effect transistor for memory cell selection; (b) depositing an insulating film on the semiconductor substrate so as to cover a surface of the plurality of word lines; (c) filling a trench formed between the plurality of word lines up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (d) filling a remaining depth portion of said trench into which the first insulating film is filled trench into which the first insulating with a second insulating film deposited by a chemical vapor deposition method; (e) punching a hole on the insulating film and the first and second insulating films between the adjacent plurality of word lines so as to reach to a pair of semiconductor regions of the field effect transistor for memory cell selection;

(f) forming a bit line electrically connected to one semiconductor region of said pair of semiconductor regions of the field effect transistor for said memory cell selection through the hole; and (g) forming an information storage capacitor element electrically connected to the other semiconductor region of said pair of semiconductor regions of the field effect transistor for memory cell selection through the hole, the step of punching a hole on the insulating film and said first and second insulating films comprising the steps of: performing etching processing on the insulating film and said first and second insulating films by having a relatively large etching selection ratio between the insulating film and the first and second insulating films and under condition that the first and second insulating films are easier to be etched and removed than the insulating film, and then performing etching processing on the insulating film and the first and second insulating films under condition that the insulating film is easier to be etched and removed than the first and second insulating films. See embodiment. (Claim 13 is suggested.)

VIII. A method for manufacturing a semiconductor integrated circuit device comprising the steps of: (a) forming an isolation trench in an isolation region of a semiconductor substrate; (b) filling the isolation trench up to predetermined middle position in its depth direction with a first insulating film deposited by a coating method; (c) filling a remaining depth portion of the isolation trench into which the filling the isolation trench up to predetermined middle position in its depth first insulating film is filled with a second insulating film; (d) forming a plurality of patterns on said semiconductor substrate after step (c); (e) filling a trench forming between the plurality of patterns up to predetermined middle position in a trench depth direction with a third insulating film

deposited by a coating method; (f) filling a remaining portion of the trench into which the third insulating film is filled with a fourth insulating film being more difficult to etch than the third insulating film; and g) forming a hole on said semiconductor substrate by etching the fourth insulating film and the third insulating film. (h) filling a conductive layer into the hole; (i) after step (h), forming a fifth insulating film on the fourth insulating film and the conductive layer; and (j) forming a hole exposing said conductive layer in the fifth insulating film by etching the fifth insulating film. See embodiment. (Claim 35 is suggested.)

IX. A semiconductor integrated circuit device, wherein an isolation portion formed in an isolation region of a semiconductor substrate includes an isolation trench dug in the isolation regions with relatively different planer dimensions, respectively in a thickness direction of said semiconductor substrate, a first insulating film formed by a coating method such that said isolation trench is filled up to predetermined middle position of its depth direction, and a second insulating film formed by a chemical vapor deposition method so as to fill a remaining depth portion of said isolation trench into which the first insulating film is filled. See embodiment. (Claim 18 is suggested.)

X. A semiconductor integrated circuit device comprising isolation regions with relatively different planar dimensions arranged on a main surface of a semiconductor substrate, an isolation trench dug in said isolation regions with relatively different planar dimensions, respectively ma thickness direction of said semiconductor substrate, a first insulating film formed by a coating method such that the isolation trench is filled up to predetermined middle position of its depth direction, and a second insulating film formed by a chemical vapor deposition method so as to fill a remaining depth portion of the

isolation trench into which the first insulating film is filled, wherein a dummy pattern is provided between the isolation trenches formed in an isolation region with a relatively large planar dimension of the isolation regions with relatively different planar dimensions. See embodiment. (Claim 19 is suggested.)

XI. A semiconductor integrated circuit device comprising a plurality of patterns adjacent to each other formed on a semiconductor substrate, a first insulating film deposited by a coating method such that a trench formed between said plurality of patterns adjacent to each other is filled up to predetermined middle position in its depth direction, and a second insulating film deposited by a chemical vapor deposition method so as to fill a remaining depth portion of the trench into which the first insulating film is filled. See embodiment. (Claims 21, 25, 26, and 28 are suggested.)

XII. A semiconductor integrated circuit device, comprising: a plurality of field effect transistors for memory cell selection formed on a semiconductor substrate; a plurality of word lines, which are wires forming a gate electrode of the field effect transistor for memory cell selection, formed adjacent to each other on a main surface of said semiconductor substrate; an insulating film on said semiconductor substrate so as to cover a surface of the plurality of word lines; a first insulating film deposited by a coating method so as to fill a trench formed between the plurality of word lines up to predetermined middle position in its depth direction; a second insulating film deposited by a chemical vapor deposition method so as to fill a remaining depth portion of the trench into which the first insulating film is filled; a hole arranged two dimensionally between the adjacent plurality of word lines and formed on the insulating film and the first and second insulating films so as to expose a pair of semiconductor regions of the

field effect transistor for memory cell selection; a bit line electrically connected to one semiconductor region of the pair of semiconductor regions of the field effect transistor for the memory cell selection through the hole; and an information storage capacitor element electrically connected to the other semiconductor region of said pair of semiconductor regions of the field effect transistor for memory cell selection through the hole. See embodiment. (Claim 22 is suggested.)

3. This application contains claims directed to the following patentably distinct species (Groups I – VIII) of the claimed invention.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record

showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. This application contains claims directed to the following patentably distinct species (Groups IX - XII) of the claimed invention.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the

case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

5. Inventions Group III and Groups IX are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case of claim 3 (Group III), instead of filling the isolation trench up to a predetermined middle position in its depth direction with a first insulating film deposited by a coating method, the first insulating film in product claim 18 (Group IX) could have been deposited by a deposition method or by heat treatment of a deposited non insulated film or selectively depositing an insulating material such as silicon dioxide on the substrate, then growing epitaxial silicon to a predetermined height between the deposited silicon dioxide, thereby creating a trench partially filled with a first insulation film of silicon dioxide. Further, invention II is distinguishable from X; invention VI is distinguishable from XI, and VII is distinguishable from XII for the same reasons.

6. Because these inventions I – XII are distinct for the reasons above, restriction for examining purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143)

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2813

November 4, 2004

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